



FEATURES

- High Pressure (100-15kpsi)
- Media Isolated –SS316 or 17-4PH
- -40-125°C (150C Avail) Operating Temperature
- Low-Profile
- 5ms Response Time
- 1% Total Error Band Pressure
- 3% Temperature Accuracy (0-70C)
- Digital Output – SPI, I2C (0x28h)
- Low-Power (<5uA Stand-by)
- IP65 (IP67 option)
- Media – Harsh Liquid, Air, & Gas

DESCRIPTION

The PPT84 is a digital (I2C, SPI) pressure and temperature transducer manufactured for a high operating temperature range for the most challenging of applications. The unique design allows for temperature measurement of the media with fast-response time. This silicon pressure transducer was designed for industrial and commercial applications. The stainless-steel design and high temperature analog component selection allows the sensor to be used in high temperature applications.

The PPT84 series utilizes MEMS piezo-resistive sensors pressurized on the passive backside of the SS housing which has superior long-term stability and accuracy (.25% Linearity).

The design is simple, cost effective, and proves reliable for OEM customers. Please contact us for Custom design availability.

APPLICATIONS

- Mil/Aero
- Industrial Automation
- HVAC
- Automotive Engine
- Compressor
- Pneumatic

Maximum Environmental Ratings

| | | | |
|---------------------------------|----------------|----------------------|------------------------|
| Operating Temperature | -40°C to 125°C | Proof pressure | 3x full scale pressure |
| Storage Temperature Range | -55°C to 130°C | Burst pressure | 5x full scale pressure |

PPT84 Digital Output Operational Characteristics

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-------------------------------|-------------|-------|--------|--------|-------|
| Supply | V_{DD} | 2.7 | 5 | 5.5 | VDC |
| Output (Option 0) | V_{OUT} | | SPI | | SPI |
| Output (Option 1) | V_{OUT} | | I2C | | I2C |
| Output (Option 2) | V_{OUT} | | RS485 | | RS485 |
| Output (Option 3) | V_{OUT} | | RS232 | | RS232 |
| Output (Option 4) | V_{OUT} | | Modbus | | PDU |
| Resolution | <i>Bits</i> | | 0.004 | | Bits |
| Linearity | $\pm\%FS$ | -0.15 | | 0.15 | %FS |
| Hysteresis | $\pm\%FS$ | -0.05 | | 0.05 | %FS |
| Repeatability | $\pm\%FS$ | -0.05 | | 0.05 | %FS |
| Temperature Error | $\pm\%FS$ | -0.15 | | 0.15 | °C |
| Accuracy (Total Error Band) | $\pm\%FS$ | -1 | 0.5 | 1 | %FS |
| Response Time | t_R | | 5 | | ms |
| Current Consumption | <i>I</i> | | 5 | | mA |
| Operating Temperature Range | °C | -40 | | 125 | °C |
| Compensated Temperature Range | °C | -20 | | 85 | °C |
| Pressure Ranges | PSI | -50 | | 15,000 | PSI |
| Proof Pressure | V_{over} | | 2X | | FS |
| Burst Pressure | V_{burst} | | 3X | | FS |
| Environmental Rating | IP | IP65 | | IP67 | IP |

Notes: 1) Measured at zero pressure. 2) Defined as best straight line 3) Measured from 0°C to 70°C 4) Over Pressure is 2x for Pressure under 10,000PSI, Burst Pressure is 3x for pressure under 5,000PSI.

Electrical Pin Configuration (Digital [SPI, I2C])



Brown/Yellow - SCL/SCLK
White - SDA/MISO
Green - INT/SS
Red - V+In
Black - GND

Fig. 2

Package

The one-piece body design is made of stainless steel (SS316L or 17-4PH), which allows for easy manufacturability and long-term stability. Automotive grade vibration proof design for engine mount.

Stability

The silicon MEMS pressure sensor element is media isolated and hermetically sealed into the SS housing. The selection of thermally capability materials reduce the mechanical stress on the sensor resulting in greater stability over time and temperature.

Additional stability is gained from factory stabilization of all sensors.

Pressure port

1/4" -18NPT and 1/8"-18NPT threads are standard SS fittings. Other port fittings such as 7/16-20UNF, and 1/4" BSP are available for OEM customers.

Media

The pressure port is tolerant to most media including but not limited to oil, air, gas, some corrosive media, and salt water.

Wetted parts

When checking media capability, the wetted surface is composed of only stainless steel (316 or 17-4).

Pressure ranges

Standard pressure ranges are 100, 300, 500, 1000, 1500, 3000, 5000, and 15,000 psi in absolute and gage. Custom pressure ranges are available for OEM customers.



2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted differential signal as well as performing temperature correction and computing the temperature value for digital output.

2.3.2. Normal Operation Mode

Two operation modes are available for normal operation: Update Rate Mode (continuous conversion at a selectable update rate) or Sleep Mode (low power). (See section 3.1.) Both modes can operate in either I2C digital output or SPI digital output. These selections are made at the factory. Factory Default is SPI.

2.3.3. EEPROM

The EEPROM array contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc.

IMPORTANT: *The EEPROM is locked at factory.*

2.3.4. Digital Interface – I2C

The IC can communicate via an addressable two-wire (I2C) interface. Commands are available for the following:

- Starting measurements in Sleep Mode
- Reading data

The PPT84 uses an I2C-compatible communication protocol with support for the bit rates listed in Table 2.7.

Table 2.7 Supported I2C™ Bit Rates

| Clock Settings | Bit Rates (Factory Set @4Mhz) |
|----------------|-------------------------------|
| 4Mhz | 400Khz or 100Khz |
| 1Mhz | 100Khz |

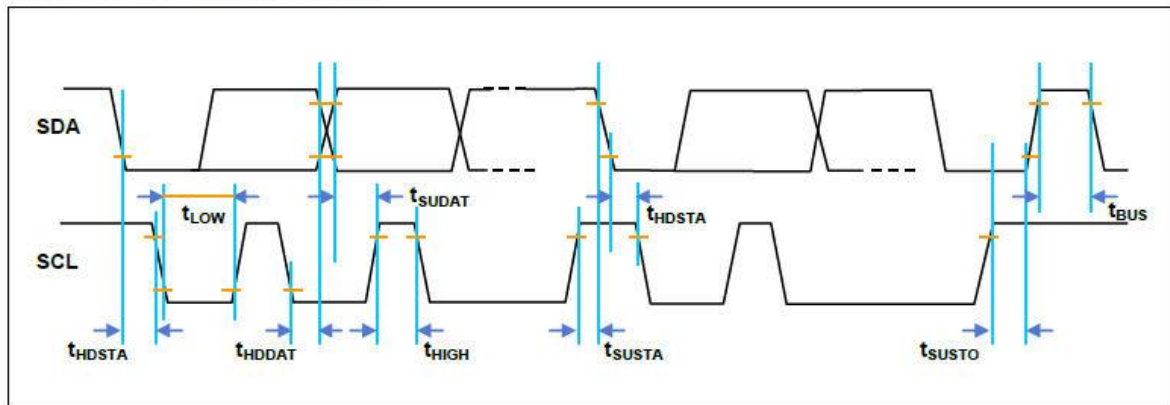
See below- Figure 2.6 for the I2C timing diagram and Table 2.8 for definitions of the parameters shown in the timing diagram.

Table 2.8 I²C™ Parameters

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|-------------|-----|-----|-----|---------|
| SCL clock frequency | f_{SCL} | 100 | | 400 | kHz |
| Start condition hold time relative to SCL edge | t_{HDSTA} | 0.1 | | | μ S |
| Minimum SCL clock low width ¹ | t_{LOW} | 0.6 | | | μ S |
| Minimum SCL clock high width ¹ | t_{HIGH} | 0.6 | | | μ S |
| Start condition setup time relative to SCL edge | t_{SUSTA} | 0.1 | | | μ S |
| Data hold time on SDA relative to SCL edge | t_{HDDAT} | 0 | | | μ S |
| Data setup time on SDA relative to SCL edge | t_{SUDAT} | 0.1 | | | μ S |
| Stop condition setup time on SCL | t_{SUSTO} | 0.1 | | | μ S |
| Bus free time between stop condition and start condition | t_{BUS} | 2 | | | μ S |

¹ Combined low and high widths must equal or exceed minimum SCL period.

Figure 2.6 I²C™ Timing Diagram



(See section 3.1 for data transmission details.)

Note: There are three differences in the PPT84 protocol when compared to standard I2C protocol:

- Sending a start-stop condition without any transitions on the CLK line (no clock pulses in between) creates a communication error for the next communication, even if the next start condition is correct and the clock pulse is applied. An additional start condition must be sent, which results in restoration of proper communication.
- The restart condition—a falling SDA edge during data transmission when the CLK clock line is still high—creates the same situation. The next communication fails, and an additional start condition must be sent for correct communication.
- A falling SDA edge is not allowed between the start condition and the first rising SCL edge. If using an I2C address with the first bit 0, SDA must be held low from the start condition through the first bit.

2.3.5. Digital Interface – SPI

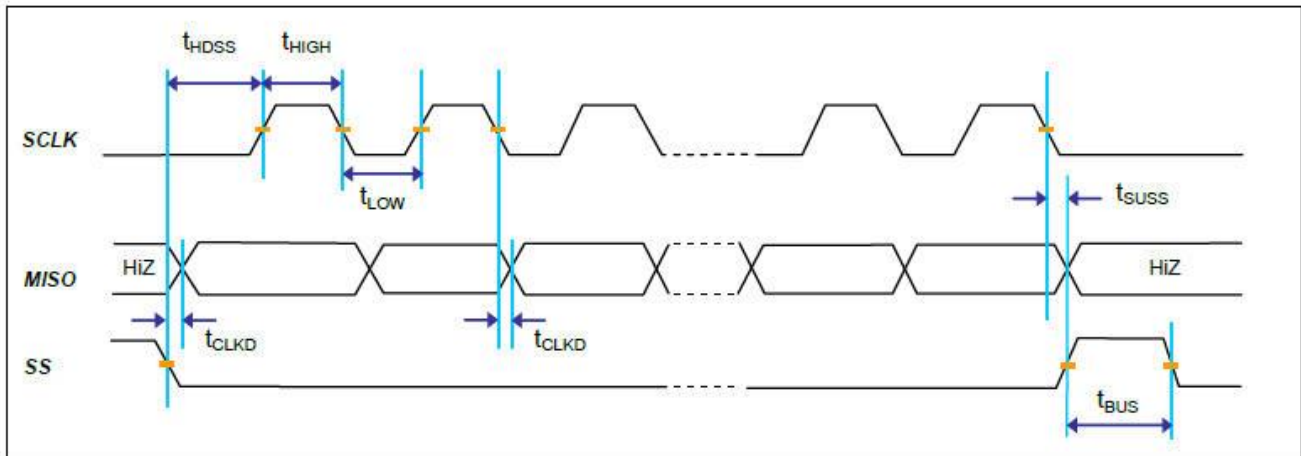
SPI is available only as half duplex (read-only from the PPT84). SPI cannot be used in the calibration environment (Command Mode) because it does not support receiving commands. SPI speeds of up to 800kHz can be supported in 4MHz Mode (200kHz in 1MHz Mode). See Figure 2.7 for the SPI timing diagram and Table 2.9 for definitions of the parameters shown in the timing diagram.

Table 2.9 SPI Parameters

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|------------|-----|-----|-----|-----------------|
| SCLK clock frequency (4MHz clock) | f_{SCLK} | 50 | | 800 | kHz |
| SCLK clock frequency (1MHz clock) | f_{SCLK} | 50 | | 200 | kHz |
| SS drop to first clock edge | t_{HDSS} | 2.5 | | | μs |
| Minimum SCLK clock low width | t_{LOW} | 0.6 | | | μs^1 |
| Minimum SCLK clock high width | t_{HIGH} | 0.6 | | | μs^1 |
| Clock edge to data transition | t_{CLKD} | 0 | | 0.1 | μs |
| Rise of SS relative to last clock edge | t_{SUSS} | 0.1 | | | μs |
| Bus free time between rise and fall of SS | t_{BUS} | 2 | | | μs |

¹ Combined low and high widths must equal or exceed minimum SCLK period.

Figure 2.7 SPI Bus Data Output Timing



(See section 3.1 for data transmission details.)

2.3.6. Clock Generator / Power-On Reset (CLKPOR)

The PPT84 has an internal 4MHz temperature compensated oscillator that provides the time base for all operations. This oscillator feeds into a 4:1 post scalar that can optionally form the clock source for the device. The FACTORY default setting is 4MHz clock digital core clock for the PPT84. If the fast response times and sampling periods provided by the 4MHz clock are not required by the customer, then the FACTORY can select the 1MHz clock which will result in better overall resolution performance.

If the power supply exceeds $\approx 1.9\text{V}$, the reset signal de-asserts and the clock generator starts working at the selected frequency (approximately 1MHz or 4MHz). The exact value only influences the conversion cycle time. To minimize the oscillator error as the VDD voltage changes, an on-chip regulator supplies the oscillator block.

2.4 Diagnostic Features

The PPT84 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. The diagnostic states are indicated by a transmission of the status of the 2 MSBs of the bridge high byte data. See Table 2.9

Table 2.9 2 MSB of Data Packet Encoding

| Status Bits (2 MSBs of Output Packet) | Definition |
|--|---|
| 00 | Normal operation, good data packet |
| 01 | Device in Command Mode |
| 10 | Stale data: Data that has already been fetched since the last measurement cycle. Note: If a data fetch is performed before or during the first measurement after power-on reset, then “stale” will be returned, but this data is actually invalid because the first measurement has not been completed. |
| 11 | Diagnostic condition exists |

When the two MSBs are 11, one of the following faults listed below is indicated.

- Invalid EEPROM signature
- Loss of bridge positive or negative
- Bridge input short
- Loss of bridge source
- Loss of bridge sink

All diagnostics are detected in the next measurement cycle and reported in the subsequent datafetch. Once a diagnostic is reported, the diagnostic status bits will not change unless both the cause of the diagnostic is fixed, and a power-on-reset is performed.

2.4.1. EEPROM Integrity

Contents of the EEPROM are protected by a 16-bit signature generated by a multiple input shift register (MISR). This signature is generated and stored in EEPROM (word 12HEX) upon leaving Command Mode if an EEPROM write has occurred. This signature is re-generated and checked for a match after Power-On-Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output. The customer ID fields (words 00HEX, 0EHEX, and 13HEX) are not included in the signature.

2.4.2. Sensor Connection Check

Four dedicated comparators constantly check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of $0.15 \cdot VDD$ to $0.85 \cdot VDD$ during all conversions. If any of the connections to the bridge break, this mechanism will detect it and put the ASIC in a diagnostic state. This diagnostic feature can be enabled/disabled with bit 0 of Diag_cfg (bits [2:1] of EEPROM word 02HEX).

2.4.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce a mid-range output signal and therefore would not be detected as a fault. If enabled via bit 1 of Diag_cfg (bits [2:1] of EEPROM word 02HEX), the sensor short diagnostic detects BP/BN shorts. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for $8\mu\text{sec}$ with a 1MHz clock or $2\mu\text{sec}$ with a 4MHz clock. System will check to see if the BN input “followed” it down below the $15\%VDD$ comparator check point. If yes, part will output a diagnostic state. Bridge has a minimum recovery time of $100\mu\text{sec}$ for 1MHz clock ($25\mu\text{sec}$ for 4MHz clock) prior to the next measurement.

3.1. General Working Mode

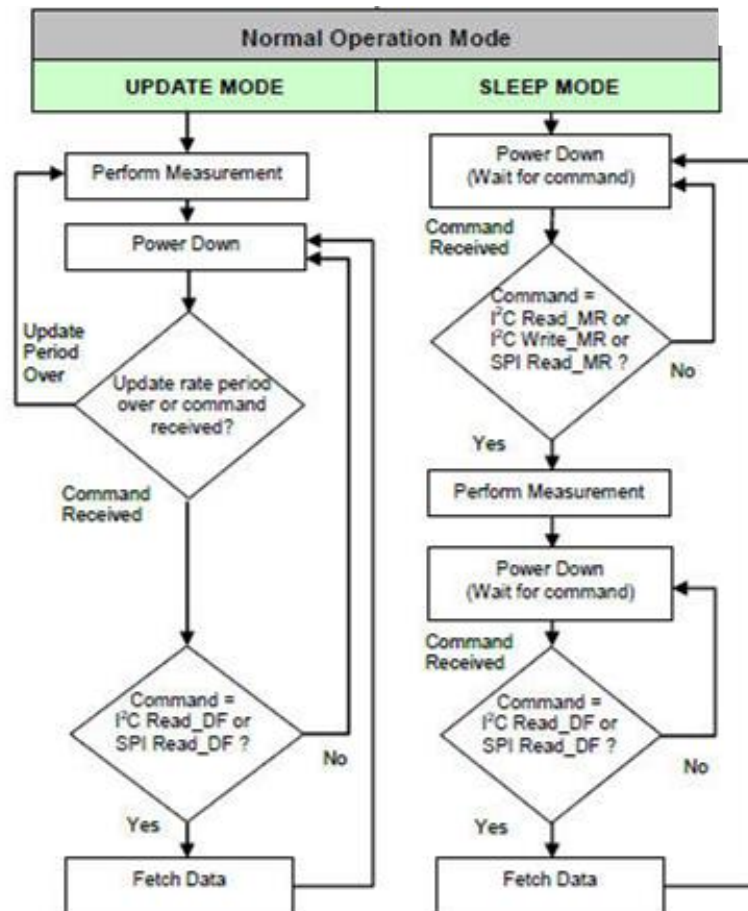
See Figure 3.1 for an overview of the general working mode of the PPT84. There are three types of commands as detailed in Table 3.1.

Table 3.1 Command Types

| Type | Description | Communication Supported | Reference Sections |
|--------------------------|--|--------------------------|----------------------------------|
| Data Fetch (DF) | Used to fetch data in any mode | I ² C and SPI | Sections 3.2.2 and 3.3.2 |
| Measurement Request (MR) | Used to start measurements in Sleep Mode | I ² C and SPI | Sections 3.1.2, 3.3.1, and 3.4.1 |

Sensor will start performing the required A2D conversions 10 milliseconds after power up. **DO NOT ISSUE ANY COMMAND DURING THIS START UP TIME.** The first corrected data will be written to the digital interface within 6ms of power-on with a 4MHz clock and the EEPROM locked.

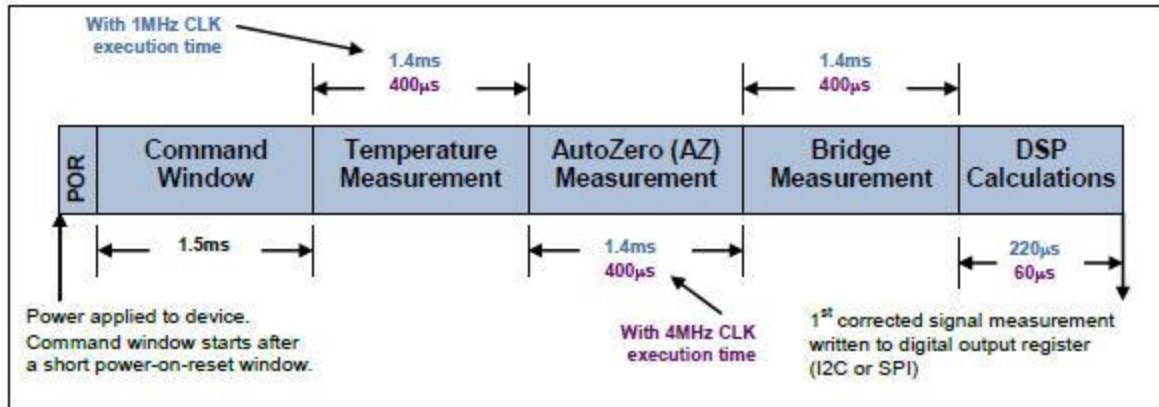
Operation after the power-on sequence depends on whether the part is programmed in Sleep Mode or in Update Mode. The factory will set up part in Sleep Mode or Update mode. In Sleep Mode, the part waits for commands from the master before taking measurements. In Update Mode, data is taken at a fixed, selectable rate. More detail is given about Update Mode and Sleep Mode in sections 3.1.1 and 3.1.2 respectively.



3.1.1. Update Mode

In Update Mode, the digital core will perform measurements and correction calculations at a selectable update rate and update the I2C/SPI output register. The power-on measurement sequence for the Update Mode is shown in Figure 3.2.

Figure 3.2 Power-Up Sequence and Timing for Update Mode with EEPROM Locked **



** When EEPROM is not locked, the command window is 4.5ms longer (= 6ms). All time values shown are typical; for the worst

If the part is programmed for the fastest update rate, conversions will continue to happen after the power-up sequence. If the PPT84 is not in the fastest update rate, the part will power down after writing to the digital output register. The duration of the power-down period is determined by the Update Rate setting (bits [7:6] in EEPROM word 01HEX; see section 3.6) and the digital core clock speed (see section 2.3.6). See Table 3.2 and Table 3.3 for the update rates. After the power-down period has expired, the PPT84 will power up; take another *bridge reading followed by calculations; write to the digital output register; and power down. Temperature and Auto-Zero (AZ) are slower moving quantities but must be updated periodically. When the part is configured in Update Mode, these two quantities are measured periodically (referred to as special measurements).*

As illustrated in Figure 3.3, valid data output to the digital register occurs after the measurement and the DSP calculations are complete. At this point the master can fetch the data in I2C or SPI with a Read_DF command. Specifics of the Read_DF command are given in sections 3.2 and 3.3. After a valid output has been read by the master, the status bits are set to “stale,” indicating that the measurement has not been updated since the last Read_DF. This mode allows the application to simply read the digital output at any time and be assured the data is no older than the selected update period. See Table 2.10 for more information on the status bits. The chip should be polled at a frequency slower than 20% more of the update rate period listed in Table 3.2 and Table 3.3.

In I2C Mode only, the INT/SS pin will assume the INT (interrupt) function. Instead of polling until a “valid” response is received, the application can look for a rise on the INT pin. This will indicate that the measurement and calculations are complete and new valid data is ready to be read on the I2C interface.

Update Rate Settings

Table 3.2 Update Rate Settings (Normal Integration Mode: 9 Coarse + 5 Fine) ¹

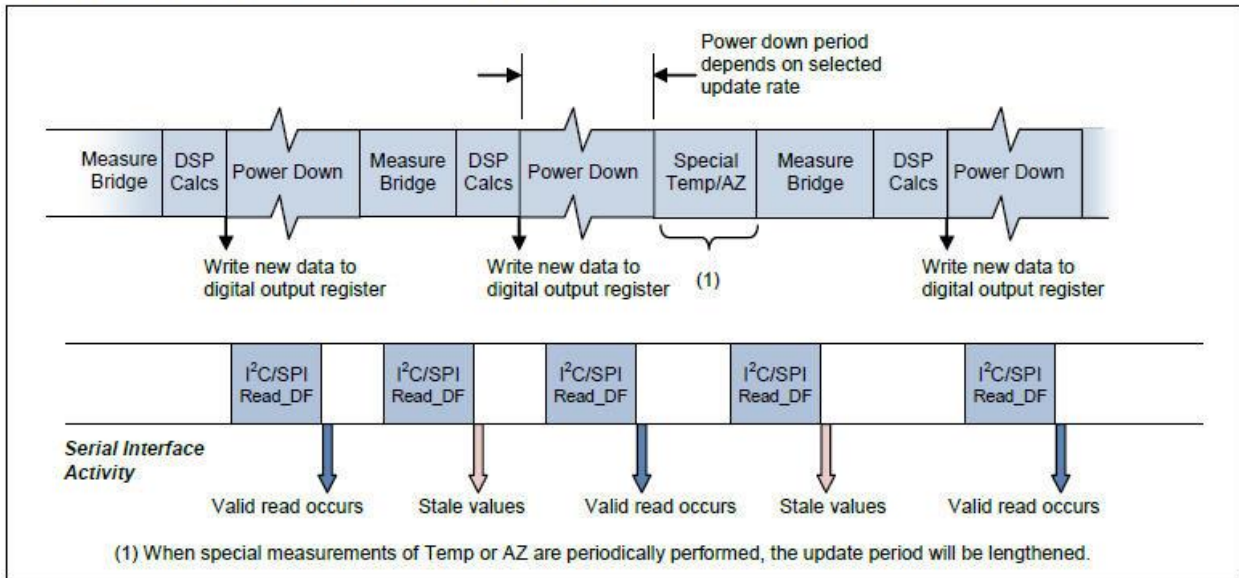
| Update_Rate | Update Period/1MHz Clock | Update Period/4MHz Clock | Measurement Cycles between Special Measurements (Temperature or AZ) |
|-----------------|--------------------------|--------------------------|---|
| 00 ² | 1.6ms | 0.5ms | 255 |
| 01 | 5.0ms | 1.5ms | 127 |
| 10 | 25.0 ms | 6.5ms | 31 |
| 11 | 125.0ms | 32.0ms | 15 |

¹ All time values shown are typical; for worst case values, multiply by 1.15 (nominal frequency $\pm 15\%$).

² With the fastest update rate setting, there is no power down period between measurements.

Factory setting will be Update_Rate 00 with an update period of .5ms. This value can be adjust by request.

Figure 3.3 Measurement Sequence in Update Mode



The benefit of slower update rates is power savings. If the update period is increased, the device will be powered down for longer periods of time, so power consumption will be reduced. When a special measurement occurs, a BP/BN (bridge) measurement will occur directly afterward. The update period during this special measurement will be increased by one conversion time over the standard measurement period.

Sleep Mode

In Sleep Mode, after the command window, the PPT84 will power down until the master sends a Read_MR (either I2C or SPI) or a Write_MR (I2C only). Specifics on the Read_MR and Write_MR commands are given in sections 3.2.1, 3.3.1, and 3.4.1. A Read_MR or Write_MR wakes the PPT84 and starts a measurement cycle. If the command is Read_MR, the part performs temperature, auto-zero (AZ), and a bridge measurement followed by the DSP correction calculations (see Figure 3.4). If the command is Write_MR, the part measures only the bridge and performs the correction calculations using previously measured temperature and auto-zero data (see Figure 3.5). Valid values are then written to the digital output register, and the PPT84 powers down again.

Following a measurement sequence and before the next measurement can be performed, the master must send a Read_DF command, which will fetch the data as 2, 3 or 4 bytes (see section 3.2.2), without waking the PPT84. When a Read_DF is performed, the data packet returned will be the last measurement made with the status bits set to “valid.” See Table 2.10 for more information on the status bits. After the Read_DF is completed, the status bits will be set to “stale.” The next Read_MR or Write_MR will wake the part again and start a new measurement cycle. If a Read_DF is sent while the measurement cycle is still in progress, then the status bits of the packet will read as “stale.” The chip should be polled at a frequency slower than 20% more than the Sleep Mode response times listed in Table 3.4 and Table 3.5.

Table 3.4 Sleep Mode Response Times (Normal Integration Mode: 9 Coarse + 5 Fine) 1

| Measurement Request | Response/1MHz Clock | Response/4MHz Clock |
|---------------------|---------------------|---------------------|
| Read MR | 4.5ms | 1.5ms |
| Write MR | 1.5 ms | 0.5ms |

¹All time values shown are typical; for worst case values, multiply by 1.15 (nominal frequency $\pm 15\%$).

Table 3.5 Sleep Mode Response Times (Long Integration Mode: 10 Coarse + 5 Fine) 1

| Measurement Request | Response/1MHz Clock | Response/4MHz Clock |
|---------------------|---------------------|---------------------|
| Read MR | 12ms | 4.5ms |
| Write MR | 5.5 ms | 1.5ms |

¹All time values shown are typical; for worst case values, multiply by 1.15 (nominal frequency $\pm 15\%$).

Note: Data is considered invalid from system power-on reset (POR) until the first measured data is written to the digital register. Sending an I2C Write_MR as the first command after power-on delivers invalid data; even though the status bits report it as “valid”. This is due to the correction calculations being performed with an uninitialized temperature and Auto-Zero value.

In I2C Mode only, the INT/SS pin will assume the INT (interrupt) function. Instead of polling until a “valid” response is received, the application can look for a rise on the INT pin. This will indicate that the measurement and calculations are complete, and new valid data is ready to be read on the I2C interface.

Power-On Sequence (Sleep Mode)

Figure 3.4 Power-on Sequence in Sleep Mode for I²C™ or SPI Read_MR (Typical Timing Values^{††})

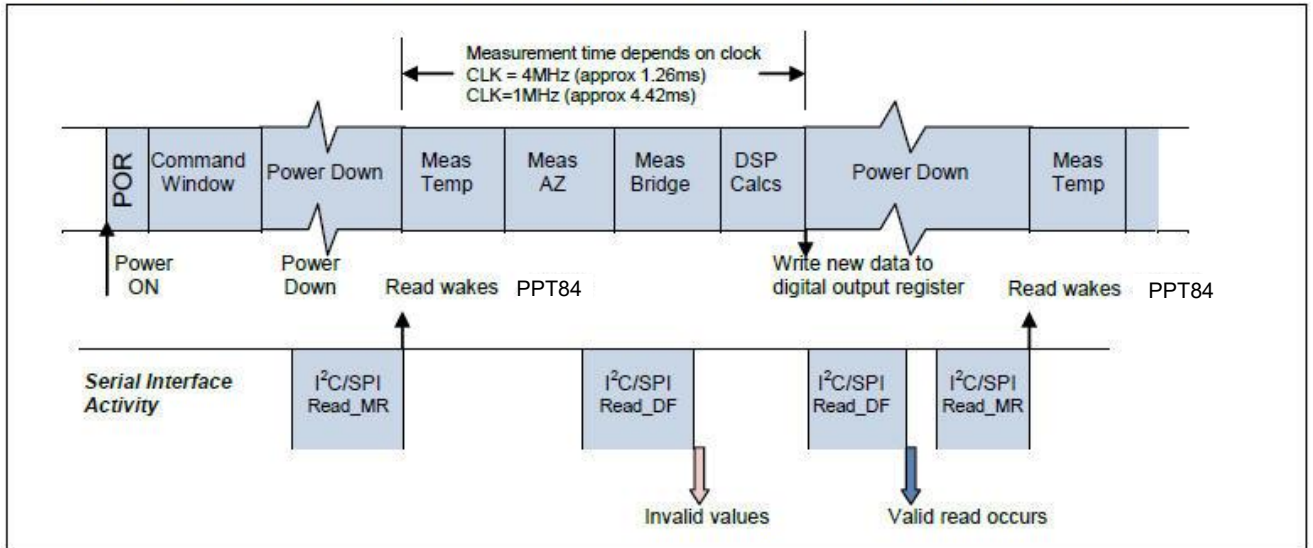
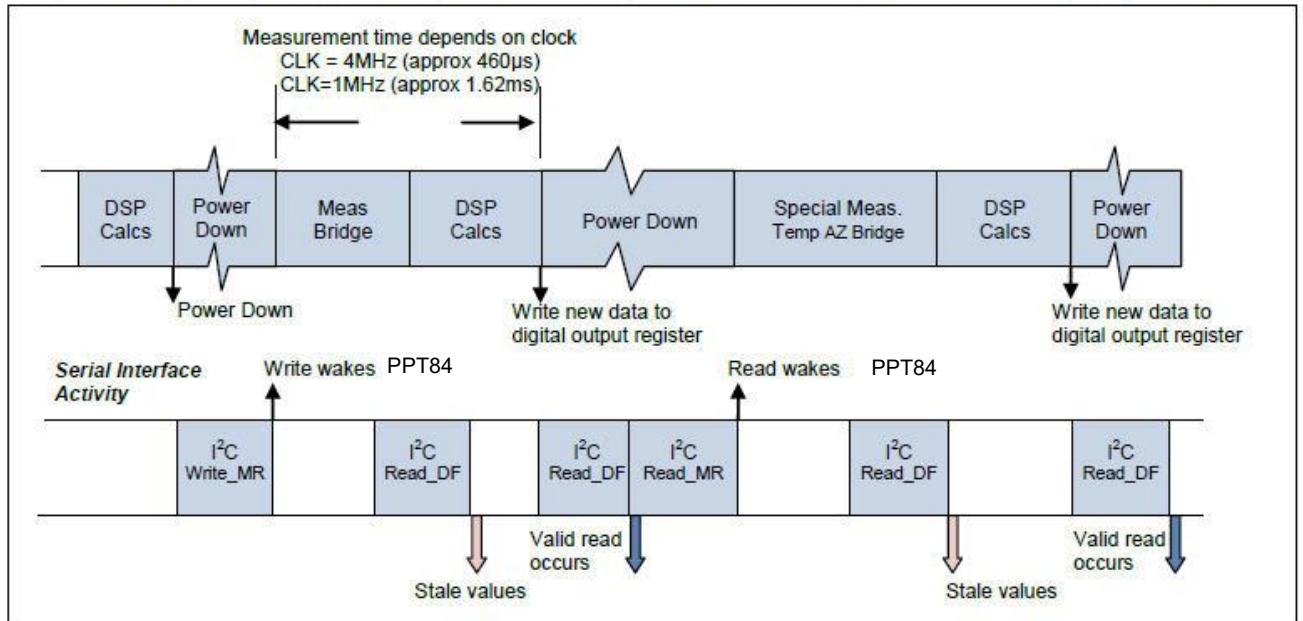


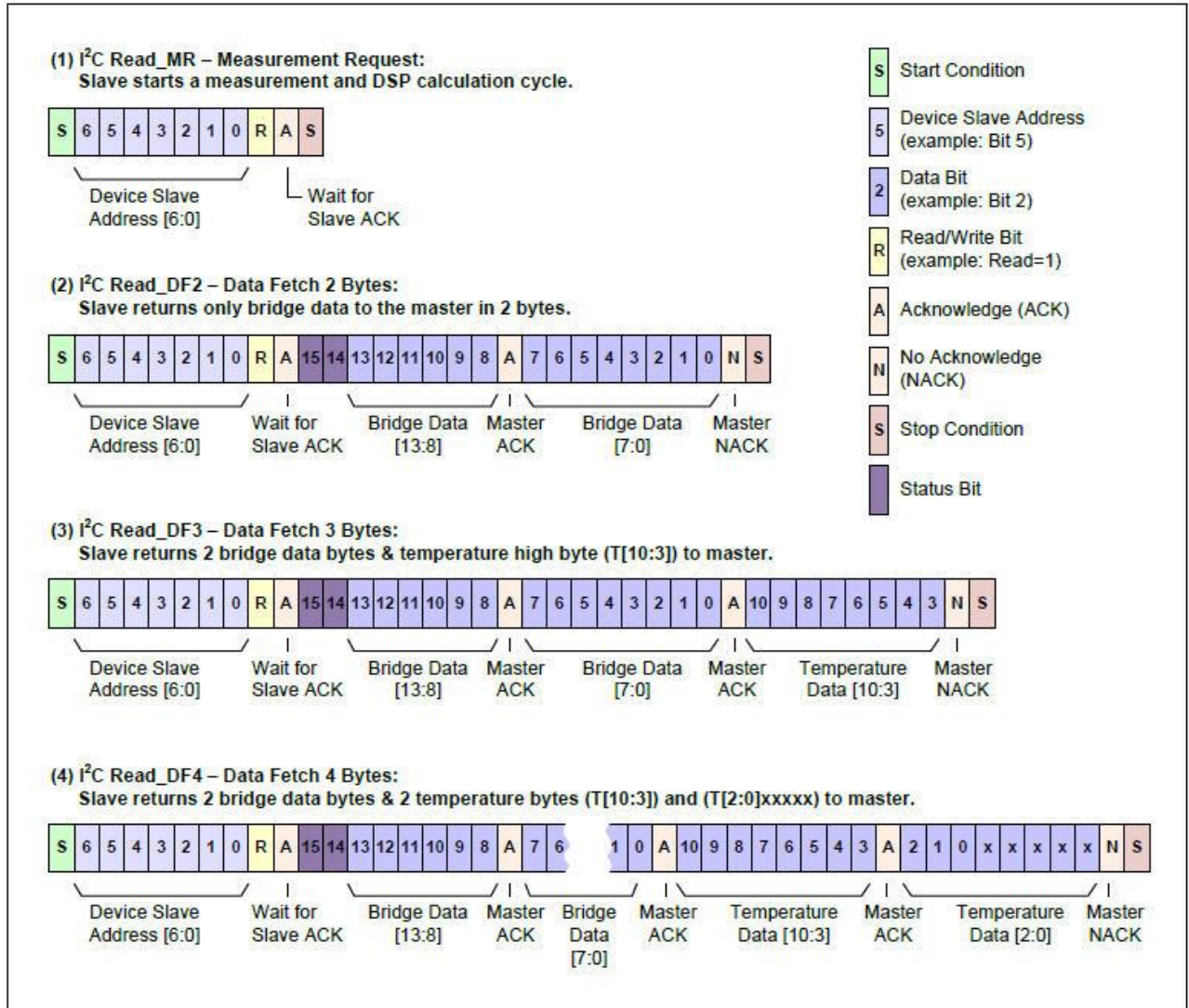
Figure 3.5 Sequence during Sleep Mode Using an I²C™ Write_MR to Wake Up (Typical Timing Values^{††})



3.2. PPT84 Read Operations with I2C™

For read operations, the I2C™ master command starts with the 7bit slave address with the 8th bit =1 (READ). The PPT84 as the slave sends an acknowledge (ACK) indicating success. The PPT84 has four I2C™ read commands: Read_MR, Read_DF2, Read_DF3, and Read_DF4. Figure 3.6 shows the structure of the measurement packet for three of the four I2C™ read commands, which are explained in sections 3.2.1 and 3.2.2.

Figure 3.6 I²C™ Measurement Packet Reads



3.2.1. I2C™ Read_MR (Measurement Request)

The Read_MR (see example 1 in Figure 3.6) communication contains only the slave address and the READ bit (1) sent by the master. After the PPT84 responds with the slave ACK, the master must create a stop condition. This is only used in Sleep Mode (see section 3.1.2) to wake up the device and start a complete measurement cycle (including the special measurements) followed by the DSP calculations and writing the results to the digital output register.

Note: The I2C™ Read_MR function can also be accomplished using the I2C™ Read_DF2 or Read_DF3 command and ignoring the “stale” data that will be returned.

3.2.2. I2C™ Read_DF (Data Fetch)

For Data Fetch commands, the number of data bytes returned by the PPT84 is determined by when the master sends the NACK and stop condition. For the Read_DF3 data fetch command (Data Fetch 3 Bytes; see example 3 in Figure 3.6), the PPT84 returns three bytes in response to the master sending the slave address and the READ bit (1): two bytes of bridge data with the two status bits as the MSBs and then 1 byte of temperature data (8-bit accuracy). After receiving the required number of data bytes, the master sends the NACK and stop condition to terminate the read operation.

For the Read_DF4 command, the master delays sending the NACK and continues reading an additional final byte to acquire the full corrected 11-bit temperature measurement. In this case, the last 5 bits of the final byte of the packet are undetermined and should be masked off in the application.

The Read_DF2 command is used if corrected temperature is not required. The master terminates the READ operation after the two bytes of bridge data (see example 2 in Figure 3.6).

3.3. SPI Read Operations

The SPI interface of PPT84 can be programmed for falling-edge MISO change or rising-edge MISO change (see SPI_Polarity, bit 0 of EEPROM word 02HEX, in section 3.6). **Falling-edge is the factory default.**

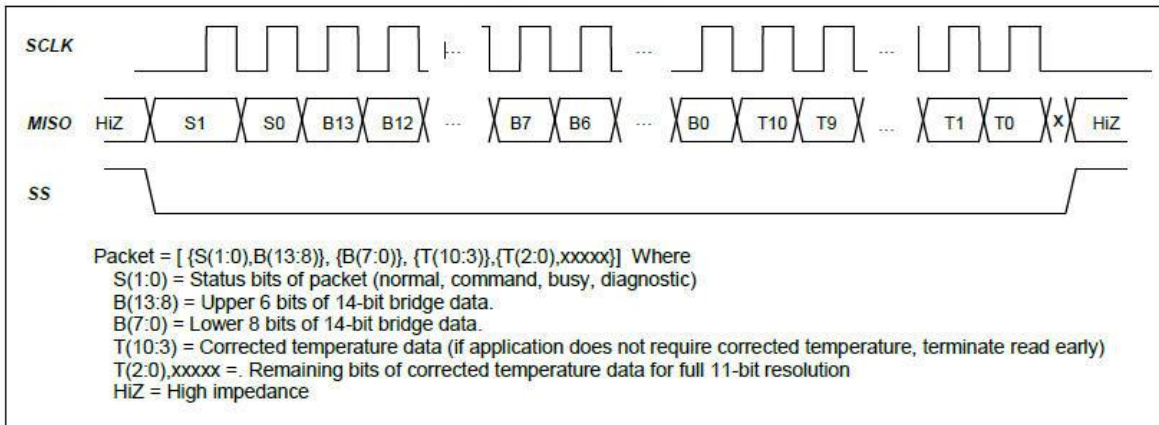
3.3.1. SPI Read_MR (Measurement Request)

A special SPI Read_MR command is used for waking up the part in Sleep Mode (see section 3.1.2). It performs a measurement cycle including the special measurements and a correction calculation. The SPI Read_MR command only requires that the SS line be dropped low for a minimum of 8µs then raised high again. The rise of SS will trigger the part to power up and perform the measurements.

3.3.2. SPI Read_DF (Data Fetch)

For simplifying explanations and illustrations, only falling edge SPI polarity will be discussed in the following sections. The SPI interface will have data change after the falling edge of SCLK. The master should sample MISO on the rise of SCLK. The entire output packet is 4 bytes (32 bits). The high bridge data byte comes first, followed by the low bridge data byte. Then 11 bits of corrected temperature (T[10:0]) are sent: first the T[10:3] byte and then the {T[2:0],xxxx} byte. The last 5 bits of the final byte are undetermined and should be masked off in the application. If the user only requires the corrected bridge value, the read can be terminated after the 2nd byte. If the corrected temperature is also required but only at an 8-bit resolution, the read can be terminated after the 3rd byte is read.

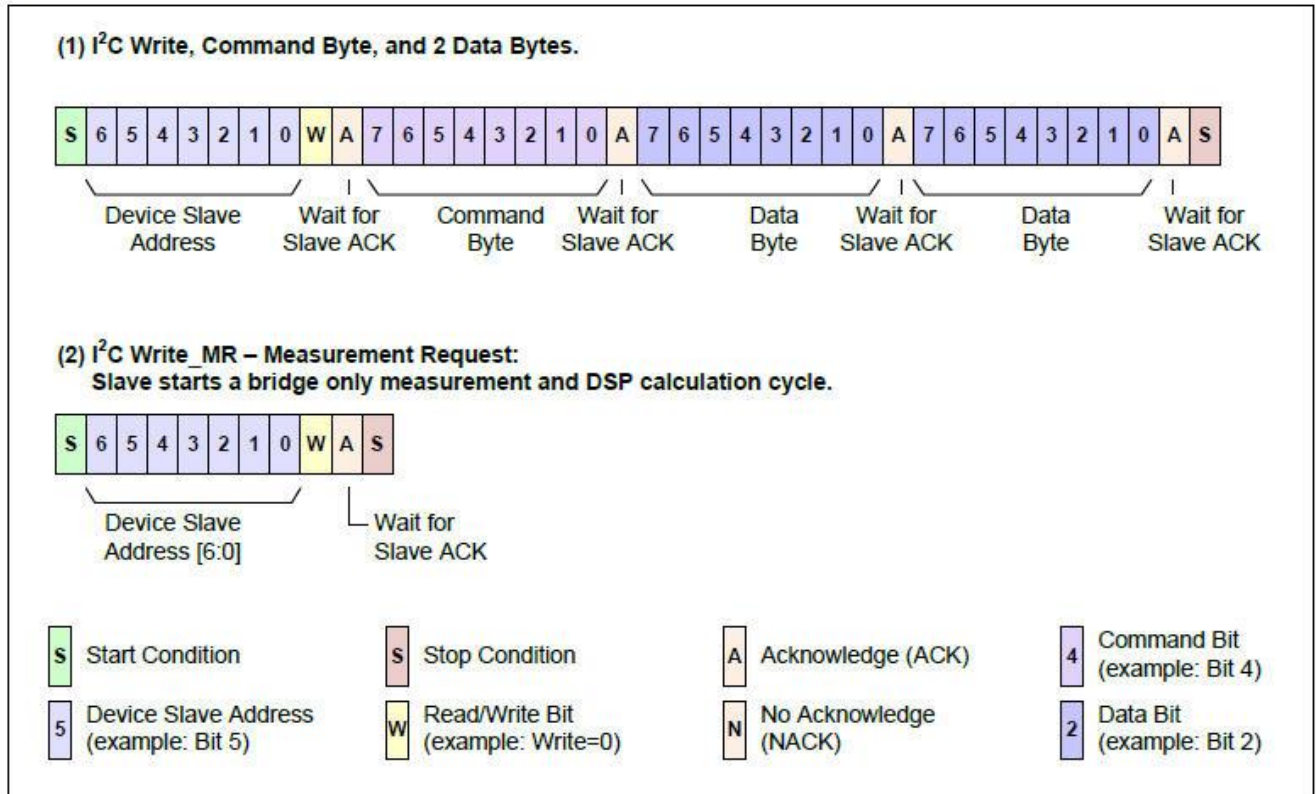
Figure 3.8 SPI Output Packet with Falling Edge SPI_Polarity



3.4. I2C™ Write Operations

For write operations, the I2C™ master command starts with the 7-bit slave address with the 8th bit =0 (WRITE). The PPT84 as the slave sends an acknowledge (ACK) indicating success. The PPT84 has two general I2C™ write command formats: I2C™ WRITE and I2C™ Write_MR. Figure 3.9 shows the structure of the write packet for the two I2C™ write commands, which are explained in sections 3.4.1 and 3.4.2.

Figure 3.9 I²C™ Measurement Packet Writes



3.4.1. I2C™ Write_MR (Measurement Request)

Write_MR is a special I2C™ write operation, which only includes the 7-bit slave address and the WRITE bit (0). This command can only be sent in Sleep Mode (see section 3.1.2). It wakes up the part and starts a measurement cycle for the bridge values only (no special measurement) and a DSP calculation based on former AZ and Temperature values. After finishing the calculation with valid results written to the digital register, the PPT84 powers down again and a Read_DF (see section 3.2.2) is required to read the valid values. See Figure 3.9 for an illustration of Write_MR.

Note: The I2C™ Write_MR function can also be accomplished using the I2C™ WRITE command with “don’t care” data in Sleep Mode.

3.4.2. Command Mode I2C™ Write Operations

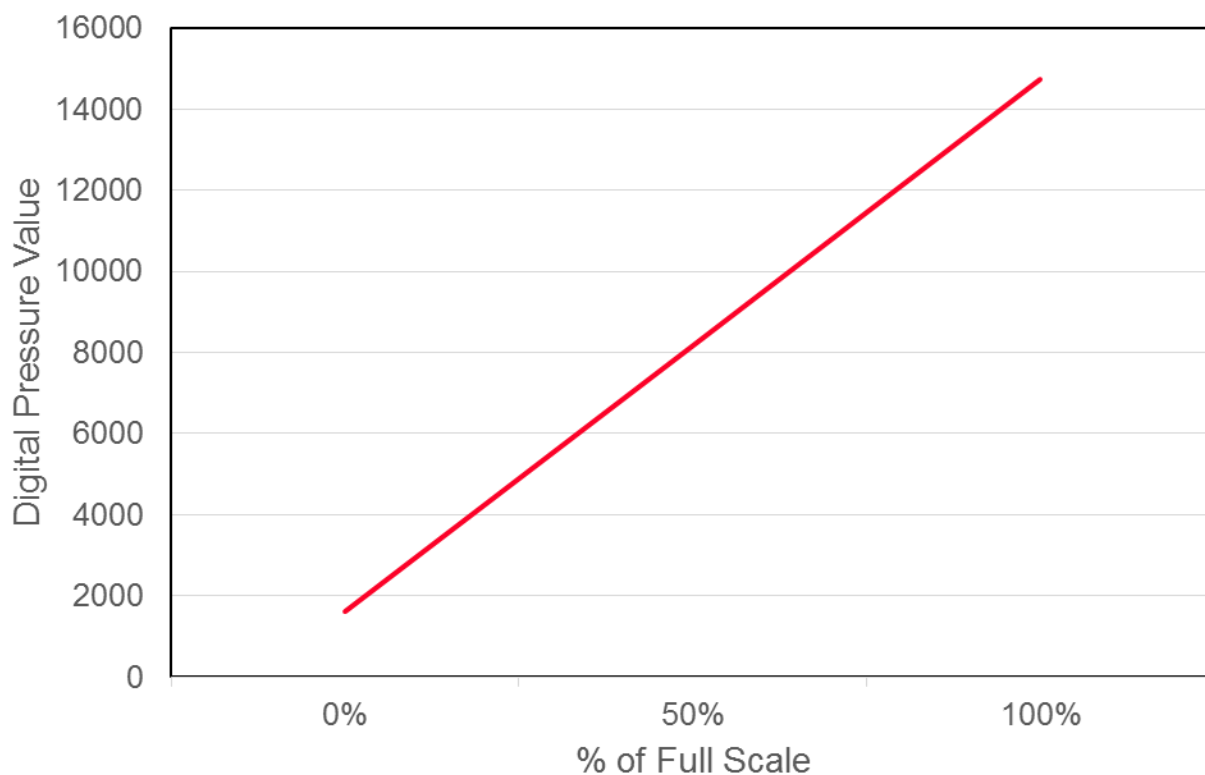
With the exception of the I2C™ Write_MR command, write operations typically only occur in Command Mode (see section 3.1) and are only supported for the I2C™ protocol. Command Mode write commands to the PPT84 are in 32-bit packets. After the write command byte (7-bit slave address followed by 0 for write), the next (2nd) byte is considered the command byte, and the subsequent two bytes form a 16-bit data field. See Figure 3.9 for an illustration of the Command Mode I2C™ WRITE command sequence.

Note: If data is not needed for the command, all zeros must be supplied as data to complete the 32-bit packet.



PPT84 Pressure / Temperature Calculation

Digital Pressure Values



Pressure Calculation Formula

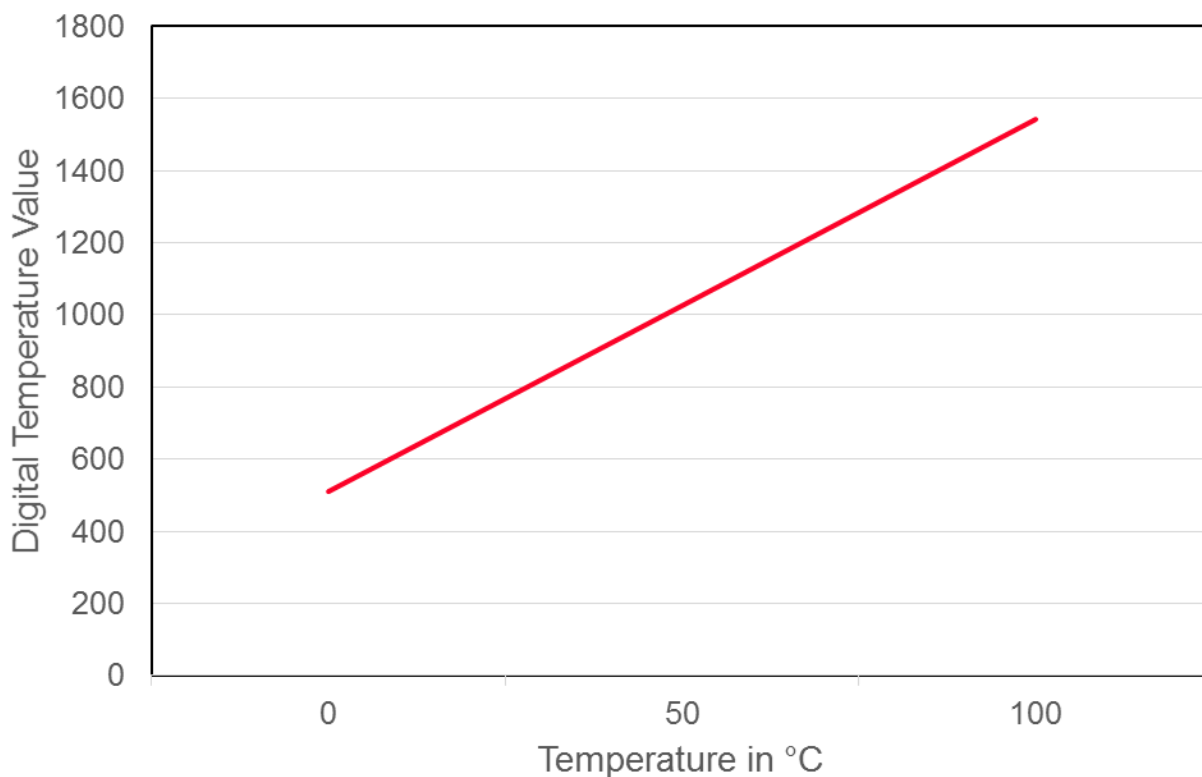
$$Y=131.25X+1638 \text{ (Offset is } \pm 125 \text{ Counts)}$$

Y= Integer Value (Counts)

X= Pressure (% of FS)



Digital Temperature Values



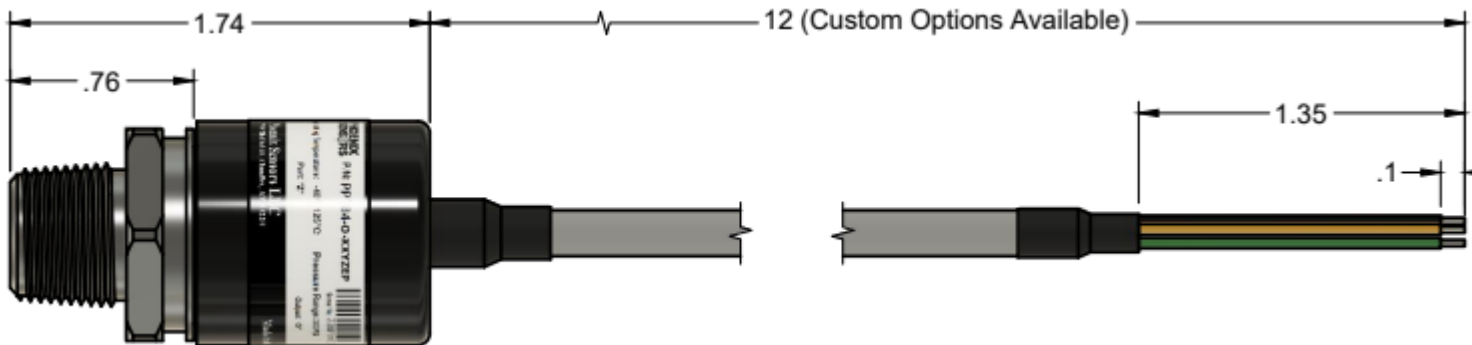
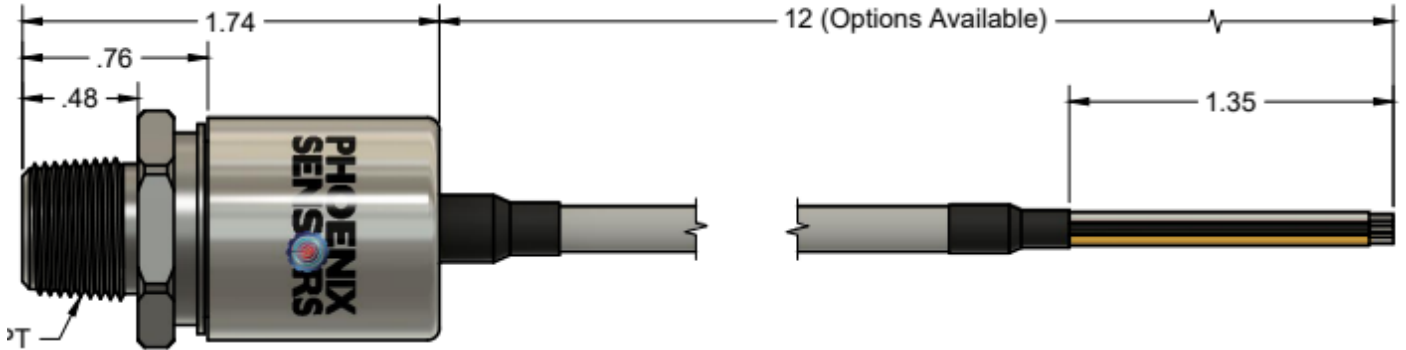
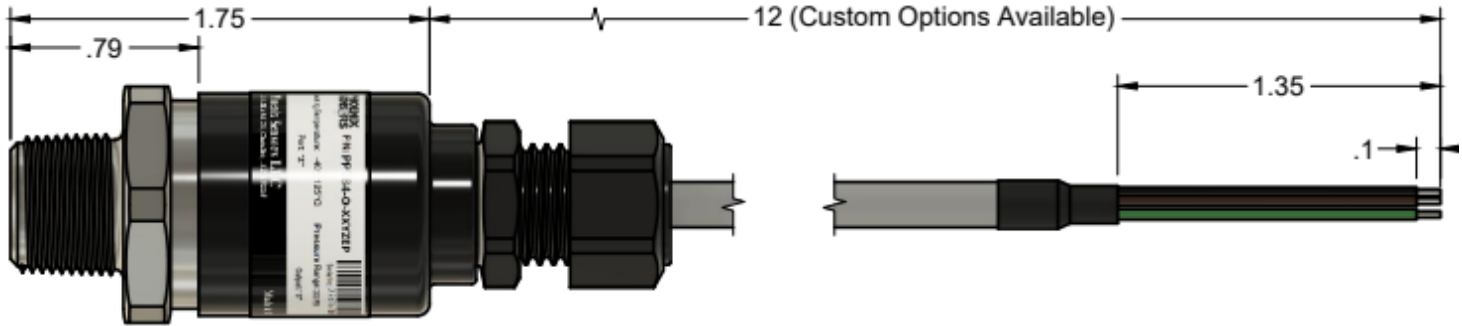
Temperature Calculation Formula

$$Y=10.3X+511 \text{ (25C = 768 Counts)}$$

Y= Integer Value (Counts)

X= Temperature (°C)

Mechanical Dimensions (inches)



NOTE: Standard Cable Length 12" (1FT)

Part Number Configuration

Phoenix Sensors Nomenclature

| Model | Output | Pressure Range | Pressure Type | Port | Environmental Rating | Power Consumption | Electrical Connection | Cable Length |
|---|------------|-----------------|-----------------------|-----------------------|----------------------|---------------------------------|--|--------------|
| PPT84 | 0 = SPI | 50 = 50 PSI | G = Gauge | 1 = 1/4" NPT Male | S = IP65 | Null = Standard (No Sleep Mode) | Null = Flying Leads (Add Cable Length) | 1 = 1FT |
| | 1 = I2C | | A = Absolute | 2 = 1/8"NPT Male | P = IP67 | L = Lower Power (Sleep Mode) | | |
| | 2 = RS485 | 15K = 15,000PSI | C = Compound (Vacuum) | 3 = 7/16"-20 UNF Male | | | | 20 = 20FT |
| | 3 = RS232 | | | 4 = 1/4" BSPP Male | | | | |
| | 4 = Modbus | | | 5 = 9/16"-18 UNF Male | | | | |
| Example: PPT84-1-50G1SL-5 I2C, 50PSI, Gauge, 1/4"NPT, IP65, Low Power (Sleep Mode), Flying Leads, 5FT Cable | | | | | | | | |

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