

PPT67 Configurable Industrial Pressure Transducer

One platform, five outputs — 0.5–4.5 V, 0–5 V, 4–20 mA, I²C or SPI · 15 to 8,000 PSI



ANALOG + DIGITAL

IP65 / IP67

MADE IN USA

DESCRIPTION

The PPT67 is a configurable industrial pressure transducer: one mechanical and electrical platform that is specified by part number for output, range, port, accuracy, temperature grade, ingress rating and cable length. OEMs standardize on a single family across analog and digital systems.

A media-isolated piezoresistive element and factory calibration deliver accuracy to $\pm 0.15\%$ FS. Digital versions write corrected pressure and temperature to an I²C or SPI register; analog versions provide a conditioned voltage or current loop. Contact us for custom configurations.

FEATURES

- Analog (0.5–4.5 V, 0–5 V, 4–20 mA) or digital (I²C, SPI) output
- Pressure ranges from 15 PSI to 8,000 PSI
- Gauge, absolute and sealed gauge references
- Accuracy options from $\pm 0.15\%$ to $\pm 1.0\%$ FS
- Three temperature grades to -40 – 125 °C
- Five standard ports incl. 9/16–18 UNF and 1/4" BSP
- Delrin or SS316L housing · IP65 or IP67
- Flying leads 1–10 ft or M8 connector
- Digital: 14-bit pressure + 11-bit temperature, Sleep Mode

APPLICATIONS

- Industrial equipment & automation
- Hydraulic & pneumatic systems
- HVAC and building systems
- Fluid & gas monitoring
- Agriculture & construction equipment
- Embedded & OEM controls

MAXIMUM ENVIRONMENTAL RATINGS

Operating Temperature	-40 to 125 °C (grade 3)
Storage Temperature	-55 to 130 °C
Ingress Protection	IP65 – IP67

Proof Pressure	1.25× full scale
Burst Pressure	1.5× full scale
Pressure Range	15 to 8,000 PSI

Operational characteristics

V+ = 5 V, V- = 0 V, T = 25 °C unless noted

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply voltage — 0.5–4.5 V, 0–5 V, digital	V _{DD}	2.7	5.0	5.5	VDC
Supply voltage — 4–20 mA	V _s	9	—	36	VDC
Output — options 0 / 1	—	0.5–4.5 V ratiometric / 0–5 V			—
Output — option 2	—	4–20 mA, two-wire			—
Output — options 3 / 4	—	I ² C (0x28) / SPI, read-only			—
Supply current — digital	I _{DD}	—	—	5	mA
Accuracy (per option)	±%FS	0.15	—	1.0	%FS
Linearity	±%FS	–0.15	—	0.15	%FS
Hysteresis	±%FS	–0.05	—	0.05	%FS
Repeatability	±%FS	–0.05	—	0.05	%FS
Temperature error	—	–1.5	—	1.5	%FS
Response time	t _R	—	5	—	ms
Operating temperature (grade 3)	T _{OP}	–40	—	125	°C
Pressure range	—	15	—	8,000	PSI

NOTES

Proof 1.25× FS · burst 1.5× FS. Grades: 1 = –10–60 °C, 2 = –20–85 °C (Delrin housing); 3 = –40–125 °C (SS316L housing).

Electrical connections

WIRE	ANALOG V	4–20 MA	I ² C	SPI
Red	V+	Supply +	VDD	VDD
Black	GND	Supply –	GND	GND
White	V _{OUT}	—	SDA	MISO
Yellow	—	—	SCL	SCLK
Green	—	—	INT	SS

26 AWG flying leads, 1–10 ft. M8 (A-coded) connector available.

Pin configuration

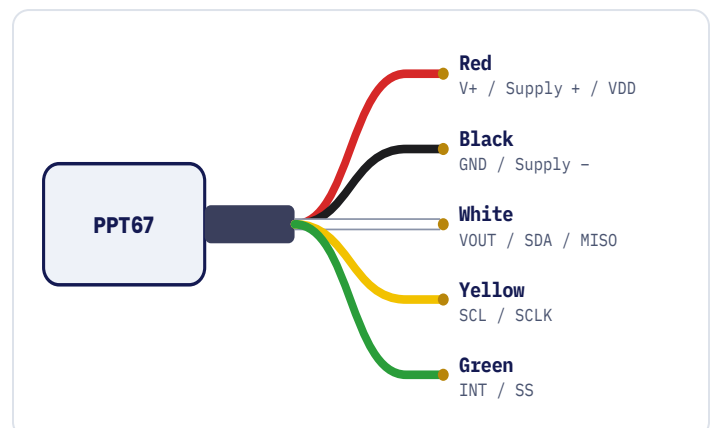


Fig. 1 – Flying-lead and M8 pinouts (PPT67 Series drawing rev A).

Application information

Package

Configuration A (15–1,000 PSI): Ø0.93" body, 1.06" hex.
Configuration B (above 1,000 PSI): extended body with cord grip. Delrin housing for grades 1–2; SS316L for grade 3 and above 85 °C.

Pressure ports

1/4" NPT, 1/8" NPT, 7/16–20 UNF–2A, 9/16–18 UNF–3A (AN) and 1/4" BSPP; custom fittings available. UNF and BSPP ports seal with a Buna-N 70 O-ring.

Wetted parts

SS316L with a Buna-N O-ring where applicable.

Stability

A media-isolated silicon piezoresistive element; material selection minimizes mounting and thermal stress. Calibration coefficients are locked in EEPROM at the factory.

Media

Oil, air, gas, water and most industrial fluids. Verify compatibility of aggressive media against the wetted materials.

Pressure ranges

15–500 PSI gauge or absolute; 250–8,000 PSI sealed gauge. Custom ranges for OEM applications.



±0.15%

Best accuracy FS

8,000

Max range PSI

5

Output options

125 °C

Max operating temp

Analog output — options 0, 1 and 2

Analog PPT67 versions provide a conditioned output proportional to applied pressure. Voltage options use three wires; the 4–20 mA option is a two-wire current loop.

Option 0 — 0.5–4.5 V ratiometric

$$V_{OUT} = V_{DD} \times (0.1 + 0.8 \times P / P_{FS})$$

At $V_{DD} = 5\text{ V}$: $V_{OUT} = 0.5\text{ V} + 4.0\text{ V} \times P / P_{FS}$

Option 1 — 0–5 V

$$V_{OUT} = 5.0\text{ V} \times P / P_{FS}$$

Option 2 — 4–20 mA

$$I_{OUT} = 4\text{ mA} + 16\text{ mA} \times P / P_{FS}$$

Hookup

WIRE / PIN · FUNCTION	CONNECT TO
Red · V+	Supply + (2.7–5.5 V; 9–36 V for 4–20 mA)
Black · GND	Supply – / loop return
White · V _{OUT}	ADC or meter input (voltage options)

Typical output

% OF FS	100 PSI	5K PSI	OPT. 0	OPT. 2
0%	0	0	0.50 V	4.0 mA
25%	25	1,250	1.50 V	8.0 mA
50%	50	2,500	2.50 V	12.0 mA
75%	75	3,750	3.50 V	16.0 mA
100%	100	5,000	4.50 V	20.0 mA

Ideal values; actual output is within the total error band.

DESIGN NOTES

Digital options 3 and 4 are described on the following pages. Keep analog leads away from switched loads; use shielded cable in electrically noisy environments.

Digital interface — I²C & SPI

A digital signal processor conditions the converted bridge signal, applies temperature correction, and computes the corrected temperature value. Calibration coefficients and configuration bits — output mode, update rate, core clock, SPI polarity — are held in EEPROM, which is **locked at the factory**. Output protocol and timing are therefore fixed for a given PPT67 part number; specify them when ordering.

I²C interface

The PPT67 communicates over an addressable two-wire interface at slave address 0x28 (other addresses available on request). Commands are supported for starting a measurement in Sleep Mode and for reading data.

CORE CLOCK	SUPPORTED I ² C BIT RATES
4 MHz (factory default)	400 kHz or 100 kHz
1 MHz	100 kHz

SPI interface

SPI is half duplex and read-only — it cannot receive commands, so it is not available in the factory calibration environment. MISO data change may be programmed for the falling or rising edge of SCLK; falling edge is the factory default.

CORE CLOCK	MAXIMUM SCLK
4 MHz (factory default)	800 kHz
1 MHz	200 kHz

Clock generator & power-on reset

An internal 4 MHz temperature-compensated oscillator provides the time base for all operations, feeding a 4:1 post-scalar that can optionally source the digital core. The 4 MHz core clock is the factory default; where fast response and sampling are not required, the 1 MHz clock yields better overall resolution performance. Once the supply exceeds ≈1.9 V the reset de-asserts and the clock starts at the selected frequency; an on-chip regulator supplies the oscillator block to minimize drift with VDD.

Status bits — 2 MSBs of the output packet

BITS	DEFINITION
00	Normal operation — good data packet
01	Device in Command Mode
10	Stale data — already fetched since the last measurement cycle
11	Diagnostic condition exists (see page 8)

If a data fetch occurs before or during the first measurement after power-on reset, "stale" is returned but the data is invalid — the first measurement has not completed.

FACTORY CONFIGURATION DEFAULTS

Protocol: per output option (3 = I²C, 4 = SPI) · I²C address: 0x28 · Core clock: 4 MHz · Update_Rate 00 (0.5 ms) · SPI polarity: falling edge · Mode: Update

EEPROM is locked before shipment. Any change to protocol, address, clock, update rate, or mode must be specified at order time.

Bus parameters & timing

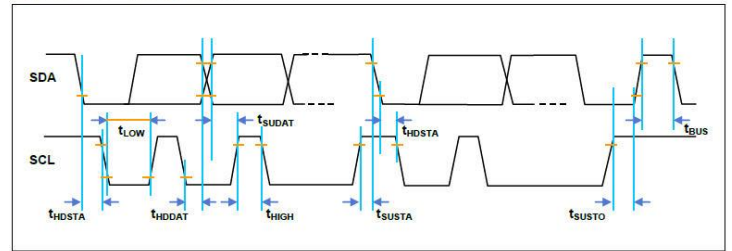
I ² C PARAMETER	SYM	MIN	MAX	UNIT
SCL clock frequency	f_{SCL}	100	400	kHz
Start condition hold time to SCL edge	t_{HSDTA}	0.1	—	μs
Minimum SCL low width	t_{LOW}	0.6	—	μs
Minimum SCL high width	t_{HIGH}	0.6	—	μs
Start condition setup to SCL edge	t_{SUSTA}	0.1	—	μs
Data hold time on SDA	t_{HDDAT}	0	—	μs
Data setup time on SDA	t_{SUDAT}	0.1	—	μs
Stop condition setup time on SCL	t_{SUSTO}	0.1	—	μs
Bus free time, stop to start	t_{BUS}	2	—	μs

SPI PARAMETER	SYM	MIN	MAX	UNIT
SCLK frequency — 4 MHz core	f_{SCL}	50	800	kHz
SCLK frequency — 1 MHz core	f_{SCL}	50	200	kHz
SS drop to first clock edge	t_{HDSS}	2.5	—	μs
Minimum SCLK low width	t_{LOW}	0.6	—	μs
Minimum SCLK high width	t_{HIGH}	0.6	—	μs
Clock edge to data transition	t_{CLKD}	0	0.1	μs
SS rise relative to last clock edge	t_{SUSS}	0.1	—	μs
Bus free time between SS rise and fall	t_{BUS}	2	—	μs

THREE DEVIATIONS FROM STANDARD I²C

- 1) A start-stop condition sent with no CLK transitions in between causes the next communication to fail, even if its start condition is correct; an additional start condition restores proper communication.
- 2) A restart condition — a falling SDA edge during data transmission while CLK is still high — creates the same failure and likewise requires an additional start condition.
- 3) A falling SDA edge is not allowed between the start condition and the first rising SCL edge. With an address whose first bit is 0, hold SDA low from the start condition through the first bit.

Figure 2.6 I²C™ Timing Diagram



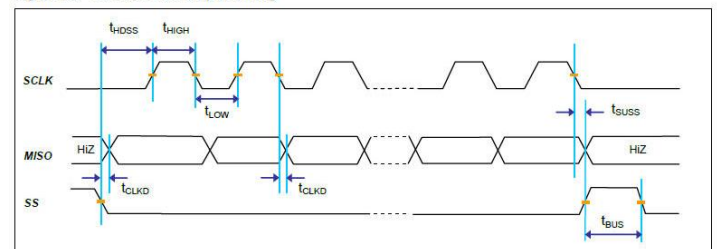
(See section 3.1 for data transmission details.)

Fig. 2 – I²C timing diagram. Combined SCL low and high widths must equal or exceed the minimum SCL period.

Rise of SS relative to last clock edge	t_{SUSS}	0.1			μs
Bus free time between rise and fall of SS	t_{BUS}	2			μs

¹ Combined low and high widths must equal or exceed minimum SCLK period.

Figure 2.7 SPI Bus Data Output Timing



(See section 3.1 for data transmission details.)

Fig. 3 – SPI bus data output timing, falling-edge polarity (factory default).

Operating modes & update rates

Conversions begin 10 ms after power-up — **do not issue any command during this start-up window**. With a 4 MHz clock and locked EEPROM, the first corrected value is written to the digital output register within 6 ms of power-on. Operation thereafter depends on whether the PPT67 is factory-programmed for Update Mode or Sleep Mode.

Update Mode

The digital core measures and corrects continuously at the selected update rate and refreshes the I²C/SPI output register. Between conversions the part powers down — slower update rates therefore save power. Temperature and auto-zero are measured periodically as special measurements; the update period lengthens by one conversion time when a special measurement occurs. The host reads the register at any time with a Read_DF and is assured data no older than the selected update period.

Sleep Mode

After the command window the part powers down and waits. A Read_MR (I²C or SPI) or Write_MR (I²C) wakes it and starts a measurement cycle: Read_MR runs temperature, auto-zero, and bridge measurements; Write_MR measures the bridge only and corrects using previously stored temperature and auto-zero data. The host then issues a Read_DF to fetch the result without waking the part again.

Figure 3.2 Power-Up Sequence and Timing for Update Mode with EEPROM Locked™

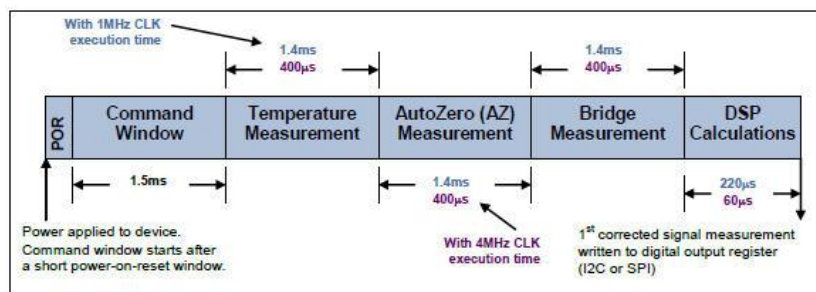


Fig. 4 – Power-up sequence and timing, Update Mode with EEPROM locked. When EEPROM is unlocked the command window is 4.5 ms longer (6 ms). Values are typical.

Update rate settings

UPDATE_RATE	PERIOD · 1 MHZ	PERIOD · 4 MHZ	CYCLES BETWEEN SPECIAL MEASUREMENTS
00 (default)	1.6 ms	0.5 ms	255
01	5.0 ms	1.5 ms	127
10	25.0 ms	6.5 ms	31
11	125.0 ms	32.0 ms	15

Normal integration mode. Typical values — multiply by 1.15 for worst case. At Update_Rate 00 there is no power-down period between measurements.

Sleep Mode response

REQUEST	1 MHZ	4 MHZ
Read_MR	4.5 ms	1.5 ms
Write_MR	1.5 ms	0.5 ms

POLLING & INT PIN

Poll no faster than 20% beyond the update period or Sleep Mode response time. In I²C mode the INT/SS pin acts as a data-ready interrupt — watch for its rise instead of polling.

Commands, data packets & conversion

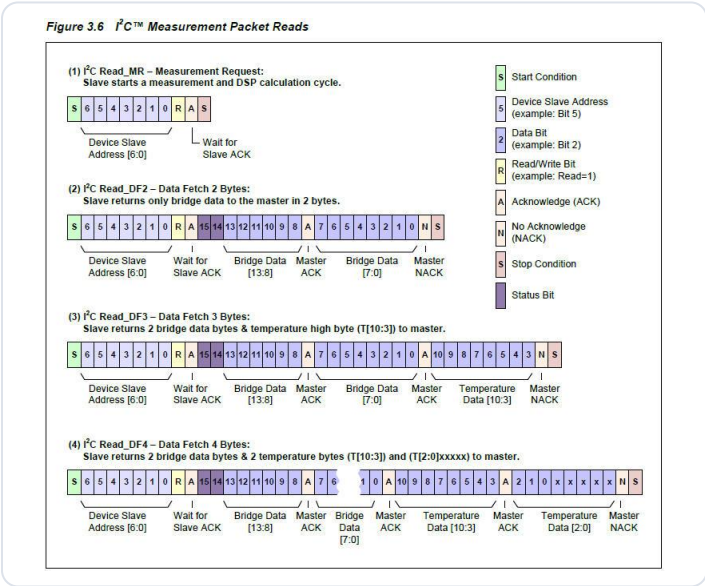


Fig. 5 – I²C measurement packet reads. The master sends the 7-bit slave address with the 8th bit = 1; the device ACKs and returns 2, 3, or 4 bytes depending on when the master sends NACK + stop.

Diagnostics

A diagnostic state is signalled when the two status MSBs read 11: invalid EEPROM signature, bridge input short, loss of bridge positive or negative, or loss of bridge source or sink. EEPROM contents are protected by a 16-bit signature re-checked at every power-on reset, and comparators verify the bridge inputs stay within 0.15·VDD to 0.85·VDD during all conversions.

COMMAND	RETURNS / ACTION	BUS
Read_MR	Wakes the part in Sleep Mode, starts a full measurement cycle	I ² C · SPI
Read_DF2	2 bytes – bridge data + 2 status MSBs	I ² C · SPI
Read_DF3	3 bytes – bridge data + 8-bit temperature	I ² C · SPI
Read_DF4	4 bytes – bridge + 11-bit temperature (mask last 5 bits)	I ² C · SPI
Write_MR	Bridge-only measurement using stored temp / auto-zero	I ² C
Command write	32-bit calibration packet – EEPROM factory locked	I ² C

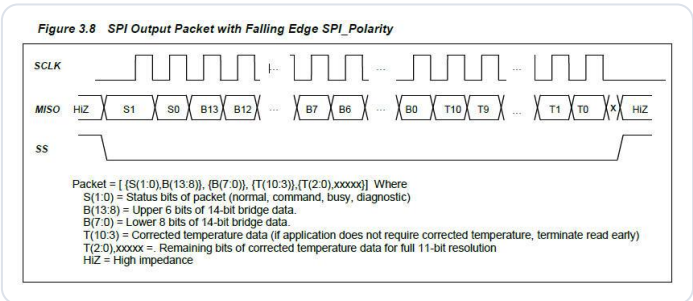


Fig. 6 – SPI output packet, falling-edge polarity. Terminate after byte 2 for pressure only, or byte 3 for 8-bit temperature.

Faults are detected in the next measurement cycle and reported in the following data fetch. Status bits will not clear until the cause is corrected **and** a power-on reset is performed.

FULL PROTOCOL REFERENCE

Command byte definitions, the EEPROM register map, Command Mode calibration sequences and long-integration timing are in the Phoenix Sensors Digital Communication Manual – available on request. Pressure and temperature conversion is on page 9.

Data conversion — pressure & temperature

Corrected pressure is returned as a 14-bit count and corrected temperature as an 11-bit count. The output is calibrated so 10% and 90% of the 14-bit span correspond to 0% and 100% of the PPT67 full-scale pressure range.

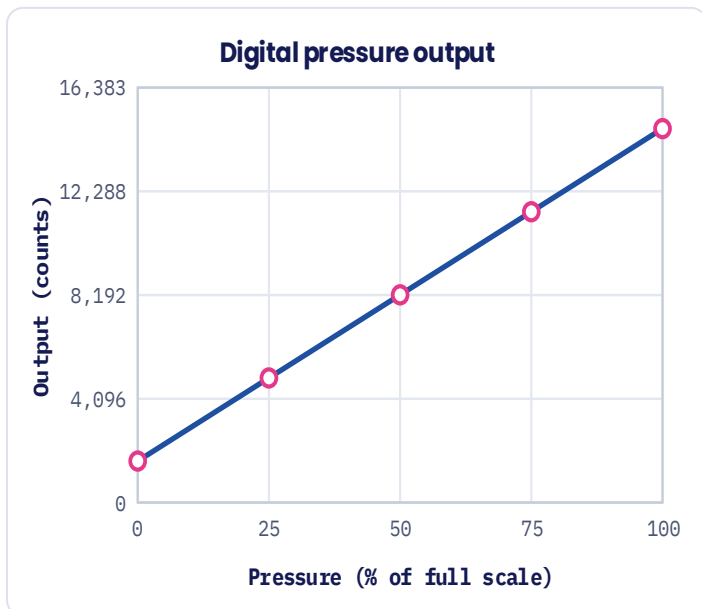


Fig. 7 – Pressure output counts vs. % of full scale.

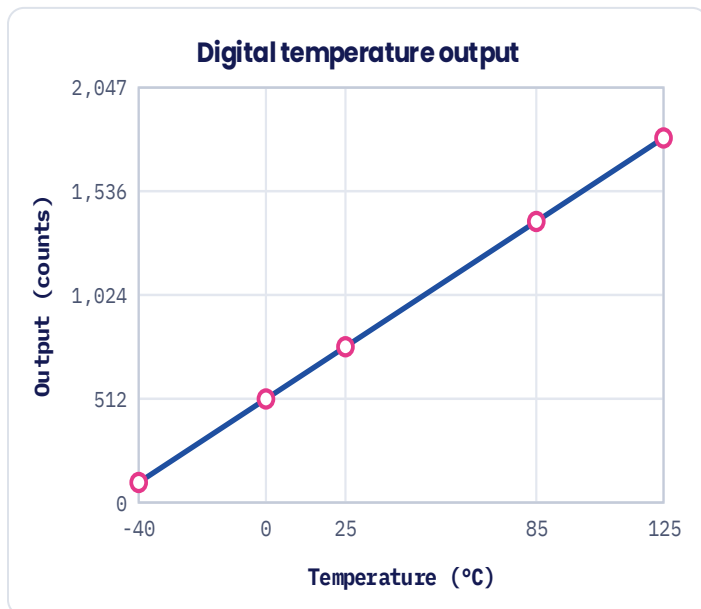


Fig. 8 – Temperature output counts vs. temperature.

Pressure counts

PRESSURE	COUNTS (DEC)	COUNTS (HEX)
0%	1,638	0x0666
25%	4,919	0x1337
50%	8,201	0x2009
75%	11,482	0x2CDA
100%	14,763	0x39AB

Temperature counts

TEMPERATURE	COUNTS (DEC)	COUNTS (HEX)
-40 °C	99	0x063
0 °C	511	0x1FF
25 °C	769	0x301
85 °C	1,387	0x56B
125 °C	1,799	0x707

CALCULATION FORMULAS

Pressure counts: $Y = 131.25 \cdot X + 1638$ (offset ± 125 counts) – X = pressure in % FS

Pressure from counts: $X = (Y - 1638) / 131.25 \rightarrow P = P_{MIN} + (P_{MAX} - P_{MIN}) \cdot X / 100$

Temperature counts: $Y = 10.3 \cdot T + 511$ (25 °C $\approx$ 768 counts) – T in °C

Temperature from counts: $T = (Y - 511) / 10.3$

Mechanical dimensions – inches [mm]

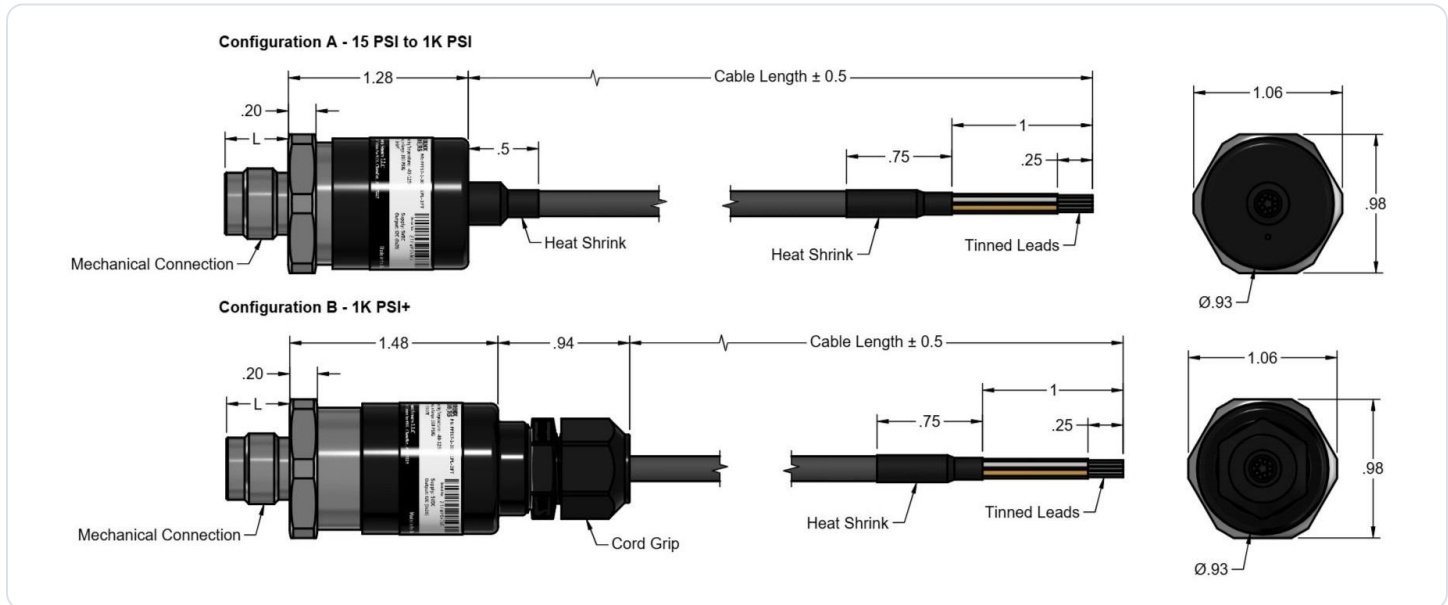


Fig. 9 – PPT67 Series outline, configurations A and B (drawing rev A, 3/17/2026).

Key dimensions

PORT	THREAD LENGTH
1 · 1/4" NPT	0.49 [12.4]
2 · 1/8" NPT	0.38 [9.7]
3 · 7/16-20 UNF-2A	0.36 [9.1]
4 · 9/16-18 UNF-3A (AN)	0.80 [20.3]
5 · 1/4" BSPP	0.51 [13.0]

Construction

Body (config. A)	$\varnothing 0.93$ [23.6] · hex 1.06 [26.9]
Height (config. A)	1.28 [32.5] + port
Config. B (above 1K PSI)	1.48 [37.6] body + cord grip
Housing	Delrin (grades 1-2) · SS316L (grade 3)
Electrical	26 AWG flying leads or M8

NOTES

IP65 standard; IP67 with cord grip or M8 connector.
Consult the outline drawing for tolerances.

Ordering information — part-number configuration

PPT67	—	0	—	15	G	1	3	1	1	—	2FT
MODEL		OUTPUT		RANGE	TYPE	PORT	ACCURACY	TEMP	IP		CABLE

OUTPUT		RANGE (PSI)		TYPE		PORT	
0	0.5–4.5 V	15–500	15, 30, 50, 100, 300, 500	G	Gauge (15–500)	1	1/4" NPT
1	0–5 V			A	Absolute (15–500)	2	1/8" NPT
2	4–20 mA	1K–8K	1K, 3K, 5K, 8K	S	Sealed (250–8K)	3	7/16–20 UNF
3	I ² C (0x28)					4	9/16–18 UNF
4	SPI					5	1/4" BSPP
						6	Custom

ACCURACY		TEMP GRADE		IP		CABLE	
1	±0.15%	1	–10–60 °C	1	IP65	1FT–10FT	Flying leads
2	±0.20%	2	–20–85 °C	2	IP67	M8	M8 connector
3	±0.25%	3	–40–125 °C				
4	±0.50%						
5	±1.00%						

DIGITAL OPTIONS — FACTORY-LOCKED SETTINGS

Core clock (4 MHz default / 1 MHz) · Update_Rate 00–11 · Operating mode (Update / Sleep) · I²C address if other than 0x28 · SPI polarity.

EXAMPLES

PPT67-0-15G1311-2FT → 0.5–4.5 V · 0–15 PSI gauge · 1/4" NPT · ±0.25% · –10–60 °C · IP65 · 2 ft leads

PPT67-4-5KS3132-8FT → SPI · 0–5,000 PSI sealed gauge · 7/16–20 UNF · ±0.15% · –40–125 °C · IP67 · 8 ft leads

Configure your PPT67

Custom ranges, addresses, update rates, fittings and cable lengths are available for OEM volumes. Talk to an engineer to spec your part.

REQUEST A QUOTE

sales@phoenixsensors.com
(480) 462-1810

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